IN THE CLAIMS

Claims 1-4 (canceled).

5. (Previously Presented) A memory integrated circuit (IC) module, comprising:

a carrier substrate;

a plurality of first and second signal connection points installed on the substrate;

a plurality of memory devices installed on the substrate, each of which has a separate memory core array and separate address decoder logic; and

a memory buffer installed on the substrate and communicatively coupled between the plurality of first and second signal connection points and the plurality of memory devices,

the buffer having a plurality of driver circuits whose outputs are coupled to the plurality of first signal connection points, respectively, and logic to a) forward read data, provided by the plurality of memory devices, at speed using the plurality of drivers in a normal mode of operation for the module and b) determine error in test symbols received from outside the module at speed using the plurality of second signal connection points in a test mode of operation for the module during which a chip-to-chip connection between the module and another device is tested.

6. (Original) The module of claim 5 wherein the carrier substrate is a printed wiring board and the plurality of memory devices are dynamic random access memory (DRAM) devices.

7. (Previously Presented) The module of claim 5 further comprising:

a plurality of third and fourth signal connection points installed on the substrate; and

wherein the buffer includes a further plurality of driver circuits whose outputs are coupled to the plurality of third signal connection points, respectively, and further logic to a) forward address and command information, that has been received from outside the module, at speed using the further plurality of driver circuits and b) determine error in test symbols, that have been received from outside the module at speed via the plurality of fourth signal connection points, in a test mode of operation

for the module during which a chip-to-chip connection between the module and another device is tested.

8. (Previously Presented) The module of claim 7 wherein the buffer is to decode local memory command, address and data, received at speed via the plurality of second signal connection points, and send them to some of the plurality of memory devices.

9. (Previously Presented) A system of integrated circuit (IC) devices, comprising:

a carrier substrate;

a host IC device having memory controller logic and installed on the substrate,

the host IC device having built-in self test (BIST) generator logic coupled between a plurality of driver circuits and the memory controller logic, to a) transmit, at speed, address and command information generated by the controller logic, using the plurality of driver circuits in a normal mode of operation for the IC device and b) transmit, at speed, test symbols, using the plurality of driver circuits in a test mode of operation for the IC device during which an interconnect between the IC device and another device is tested,

the host IC device having BIST checker logic coupled between a plurality of receiver circuits and the memory controller logic, to a) forward data, received by the plurality of receiver circuits, to the memory controller logic in said normal mode of operation for the IC device and b) determine error in test symbols received by the plurality of receiver circuits in a test mode of operation for the IC device during which an interconnect between the IC device and another device is tested; and

a first main memory module installed on the substrate to communicate with the host IC device,

the first module having a memory buffer circuit with repeater capability to a) forward address and command information from the memory controller logic to a second main memory module, and b) forward read data from the second main memory module to the memory controller logic,

the first module having first BIST checker logic to determine error in the test symbols transmitted by the BIST generator logic of the host IC device.

10. (Original) The system of claim 9 further comprising the second main memory module installed on the substrate to communicate with the host IC device through the first main memory module,

the second module to re-transmit the test symbols transmitted by the host IC device and forwarded by the first module, back to the first module.

11. (Original) The system of claim 10 wherein the first module further comprises second BIST checker logic to determine error in the re-transmitted test symbols received from the second module.

12. (Original) The system of claim 9 wherein the host IC device is a processor device that includes a processor core coupled to the memory controller logic to access the main memory modules.

13. (Original) The system of claim 9 wherein the host IC device is a system chipset device that a processor of the system uses to access the main memory modules and computer system peripherals.

Claims 14-21 (canceled).